WBS 6.7
DAQ/Data Handling

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U.S. ATLAS HL-LHC Upgrade Director's Review
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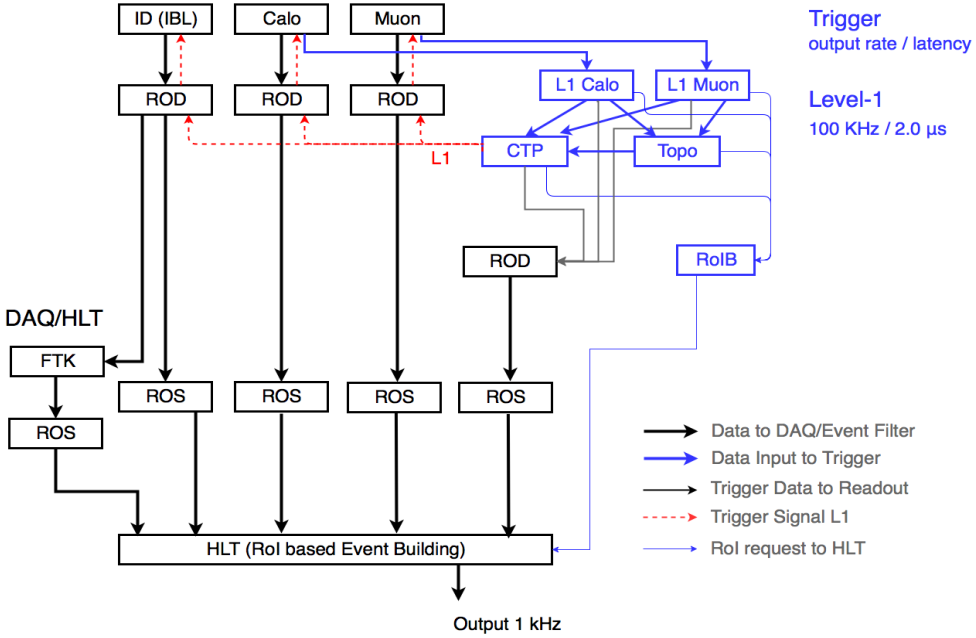
Outline

- System Overview
  - Current TDAQ System and Motivation for Upgrade
  - ATLAS TDAQ HL-LHC Upgrade Plans
- Proposed U.S. HL-LHC Upgrade Scope
  - Work Breakdown Structure and Contributing Institutes
  - U.S. Deliverables
- Ongoing R&D
  - Plans to Construction Project
- Construction Project Management
  - Construction Project Schedule and Budget
  - Risk and Contingency
- Closing Remarks

Current TDAQ System

- TDAQ system for Run 2
  - Some Phase-0 enhancements after Run 1



- Phase-I upgrades ongoing
  - Level-1 Calorimeter trigger (L1CALO) with fine granularity LAr data, Level-1 Muon trigger (L1Muon) with New Small Wheel data, Fast TracKer (FTK), new readout with Fron-End LInk eXchange (FELIX)

Motivation for HL-LHC Upgrade

Retain great TDAQ performance for the HL-LHC physics program

- Precision Higgs measurements and BSM physics searches
- Trigger and DAQ capabilities essential to physics program
  - To maintain Run 1 like trigger performance
  - To recoup trigger efficiency as needed
  - To enhance DAQ system for detector changes, higher trigger rate and larger event size
- Trigger Menu requirements
  - Low single lepton thresholds (~20 GeV) needed to fully exploit the physics program
  - Hadronic tau decays important for Higgs and new physics studies
  - Fully hadronic triggers needed for missing energy, multijets, etc for SUSY and DM studies

$\mathcal{L}=7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$

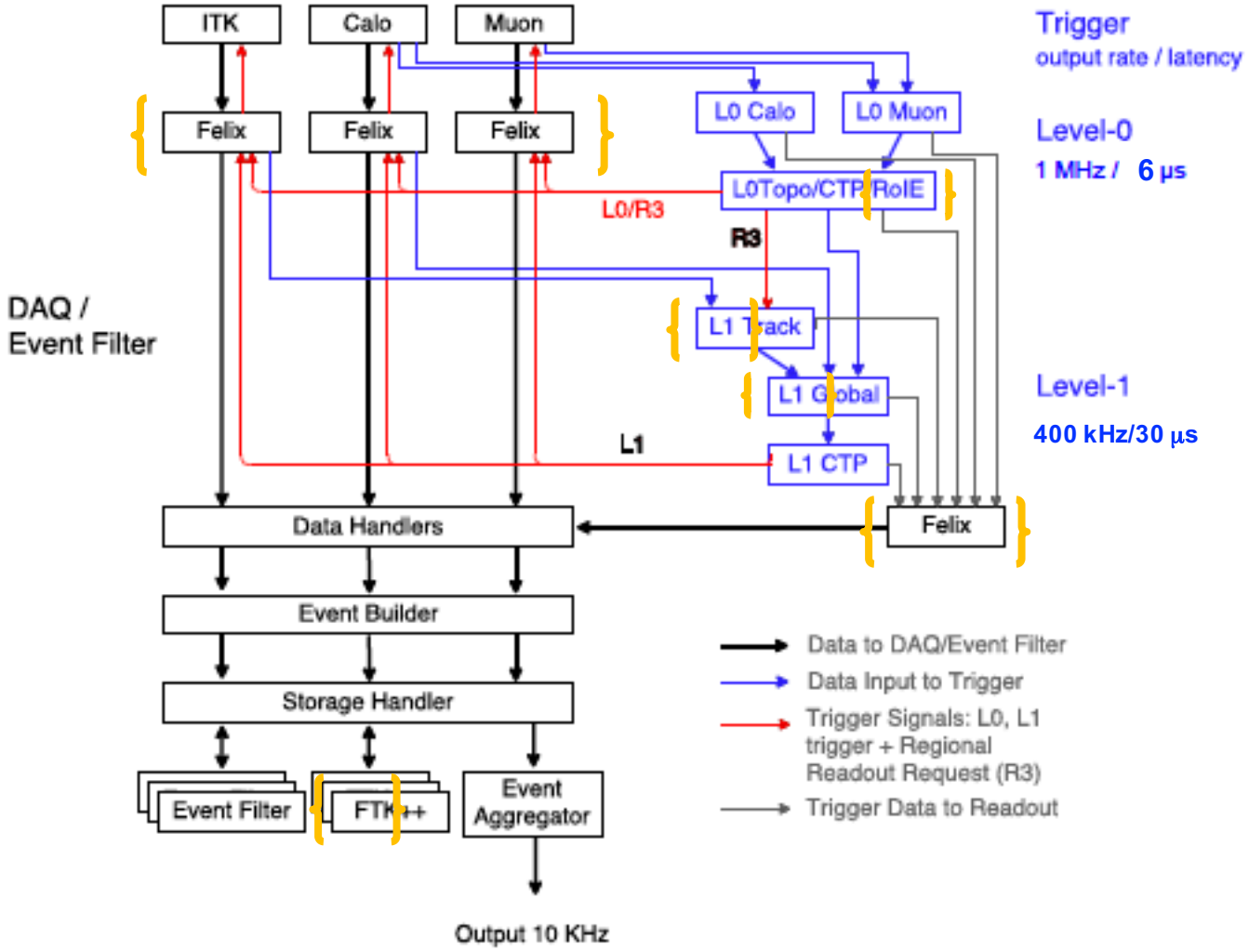
Item	Offline p_{T} Threshold [GeV]	Offline $\lvert\eta\rvert$	L0 Rate [kHz]	L1 Rate [kHz]	EF Rate [kHz]
isolated Single e	22	< 2.5	200	40	2.20
forward e	35	$2.4 - 4.0$	40	8	0.23
single γ	120	< 2.4	66	33	0.27
single μ	20	< 2.4	40	40	2.20
di-γ	25	< 2.4	8	4	0.18
di-e	15	< 2.5	90	10	0.08
di-μ	11	< 2.4	20	20	0.25
$e-\mu$	15	< 2.4	65	10	0.08
single τ	150	< 2.5	20	10	0.13
di-τ	40,30	< 2.5	200	30	0.08
single jet	180	< 3.2	60	30	0.60*
fat jet	375	< 3.2	35	20	0.35*
four-jet	75	< 3.2	50	25	0.50*
H_{T}	500	< 3.2	60	30	0.60*
$E_{\mathrm{T}}^{\mathrm{miss}}$	200	< 4.9	50	25	0.50*
jet + $E_{\mathrm{T}}^{\mathrm{miss}}$	140,125	< 4.9	60	30	0.30*
forward jet**	180	3.2 - 4.9	30	15	0.30*
Total			~1000	~400	~10

TDAQ System HL-LHC Upgrade Plans

Architecture with a two-level hardware trigger

- Split L0/L1 trigger architecture
  - Accept rate/latency: (L0: 1 MHz, 6 μs; L1: 400 kHz, 30 μs)
  - L0 reducing rate down to 1 MHz
    - Phase-I L1Calo to be HL-LHC L0Calo, new L0Muon including MDT trigger
    - Producing a list of Region of Interests (RoI) to seed the L1 selection
  - RoI based L1 reducing rate further down to 400 kHz
    - FTK-like L1Track to produce tracking information, critical for selection algorithms in high pileup environment
    - L1Global to combine tracking information, full granularity Calo data, and Muon information
  - Event Filter reducing rate further down to ~10 kHz
    - Full event tracking @ 100 kHz by FTK++, critical for selection algorithms in high pileup environment
- FELIX as new readout system to accommodate
  - Detector changes (ITk, new Calo and Muon electronics, etc)
  - Higher trigger rate (1 MHz vs 100 kHz)
  - Larger event size (5 MB vs 2 MB)

HL-LHC ATLAS TDAQ Architecture



US Interests

Proposed U.S. Scope

- DOE scope of the TDAQ system HL-LHC upgrade
- 6.7 DAQ/Data Handling: Detector readout and data preparation for trigger processing
  - L1Global Aggregator: aggregation of tracking data, full granularity Calo data and Muon information for L1Global event processing
  - L1Track/FTK++ Data Handling: high speed data transmission for L1Track/FTK++ to perform pattern match and track fitting
  - FELIX card: detector readout system in the HL-LHC phase
  - RoI Distributor: Distributing the RoIs to seed L1 for data collection and trigger selection
- Extend the expertise and experience from US ATLAS responsibilities in the original TDAQ construction and Phase-I upgrade

Proposed U.S. Deliverables

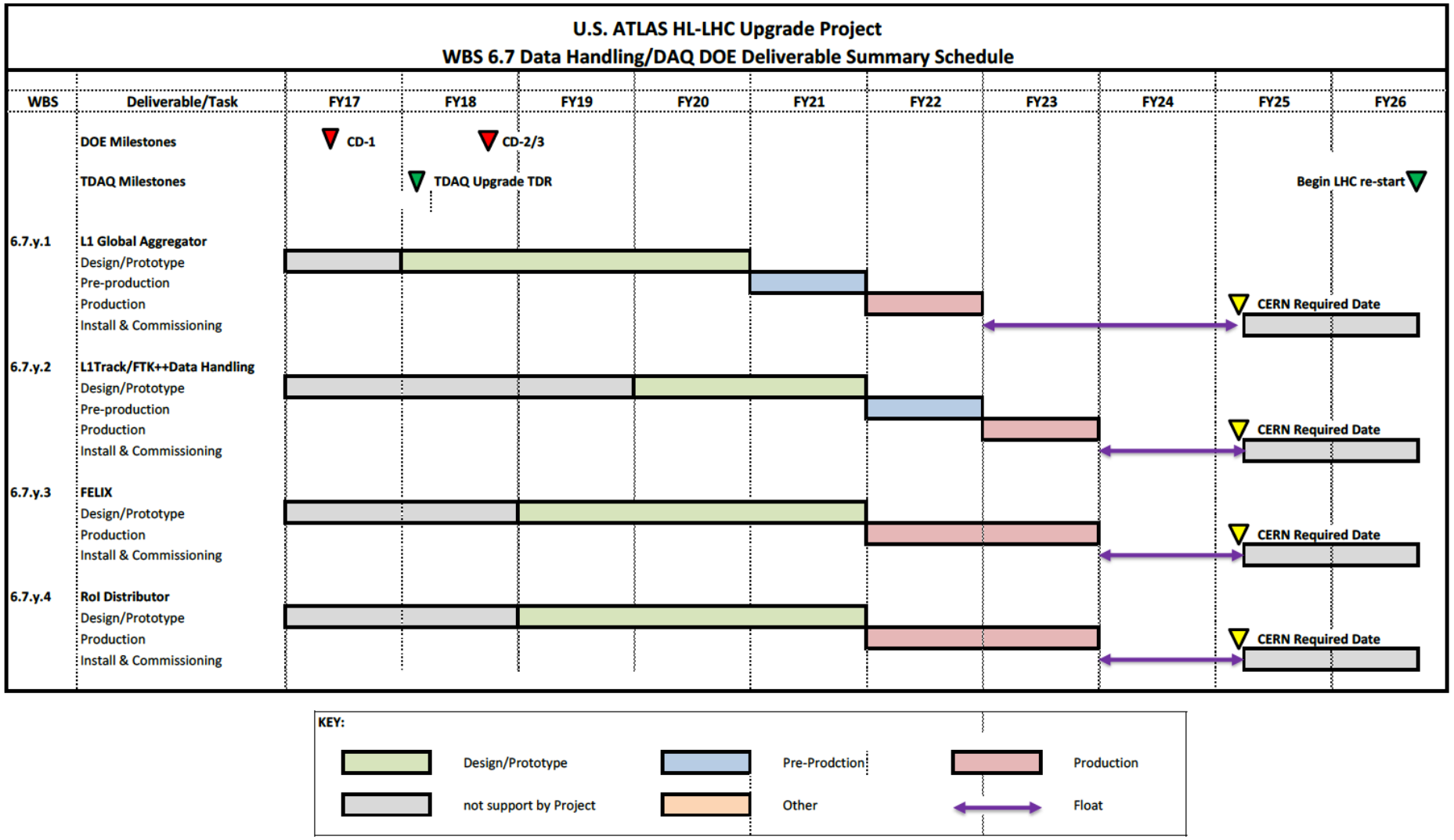
- 6.7.y.1 L1Global Aggregator
  - Design, prototype, (fractional) production and testing of the boards; firmware
  - Institute: BNL
- 6.7.y.2 L1Track/FTK++ Data Handling
  - Design, prototype, (fractional) production and testing the Real Transition Module (RTM); data transmission firmware
  - Institute: ANL, SLAC
- 6.7.y.3 FELIX
  - Design, prototype, (fractional) production and testing the FELIX cards; firmware
  - Institute: ANL, BNL
- 6.7.y.4 RoI Distributor
  - Design, prototype, production and testing the RoI Distributor boards; firmware
  - Institute: ANL

	Proposed US Contribution	Full System
L1Global Aggregator boards	4	8
L1Track/FTK++ Data Handling RTMs	697	1394
FELIX cards	70	450
RoI Distributor boards	2	2

Research & Development

- Status of ongoing R&D
  - Leverage of system evolution and Phase-I upgrade experience
    - Phase-I FELIX for FELIX
    - Phase-I gFEX for aggregator
    - Phase-I FTK for L1Track/FTK++ Data Handling
    - RoIB evolution for RoID
- Plans for R&D through start of construction (highlights)
  - To demonstrate the processing performance with high performance FPGA and high speed optical links
  - To develop the FELIX full requirements and to demonstrate the low latency transmission
  - To develop the RoI distribution requirements and mechanism
- Details in R&D presentation in the breakout session

Schedule & Milestones

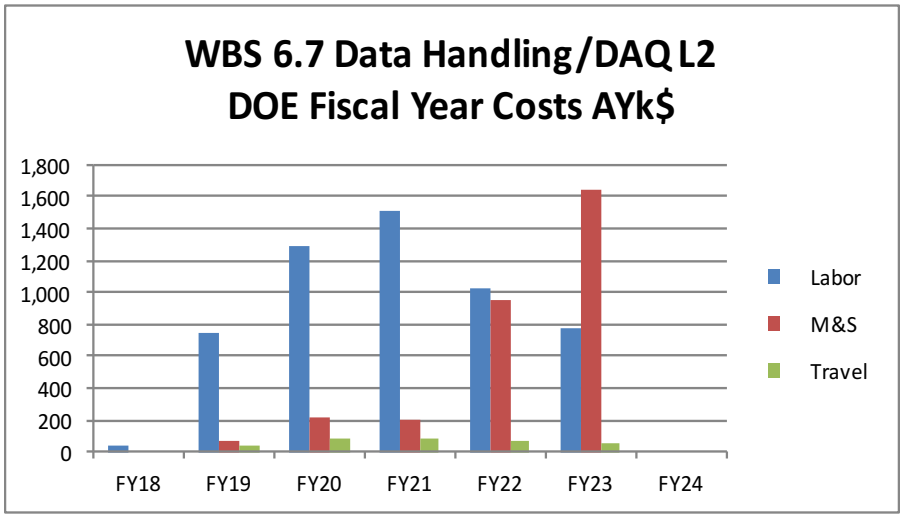


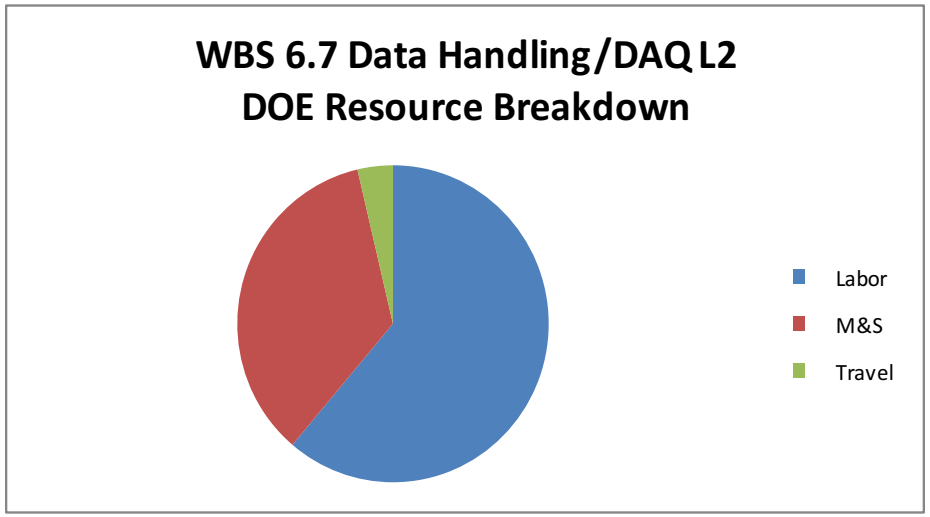
Cost and Effort Estimates

- Labor
  - Experience from Phase-I upgrade (e.g., gFEX)
  - Past ATLAS TDAQ projects
- M&S
  - Components based on quotes from vendors
  - Production hardware estimates based on recent experience with hardware for Phase-I projects
  - ATLAS scoping document as input
- Travel
  - Estimates of the number of trips needed to converge on interfaces, joint tests and reporting.

Cost and Effort

6.7 Data Handling/DAQ DOE Total Cost (AYk$)								
	FY18	FY19	FY20	FY21	FY22	FY23	FY24	Grand Total
DOE								
Labor	46	750	1,284	1,504	1,024	781	0	5,390
M&S	0	74	218	208	956	1,643	0	3,098
Travel	0	44	79	79	64	58	0	323
DOE Total	**46**	**867**	**1,581**	**1,791**	**2,044**	**2,481**	**0**	**8,811**



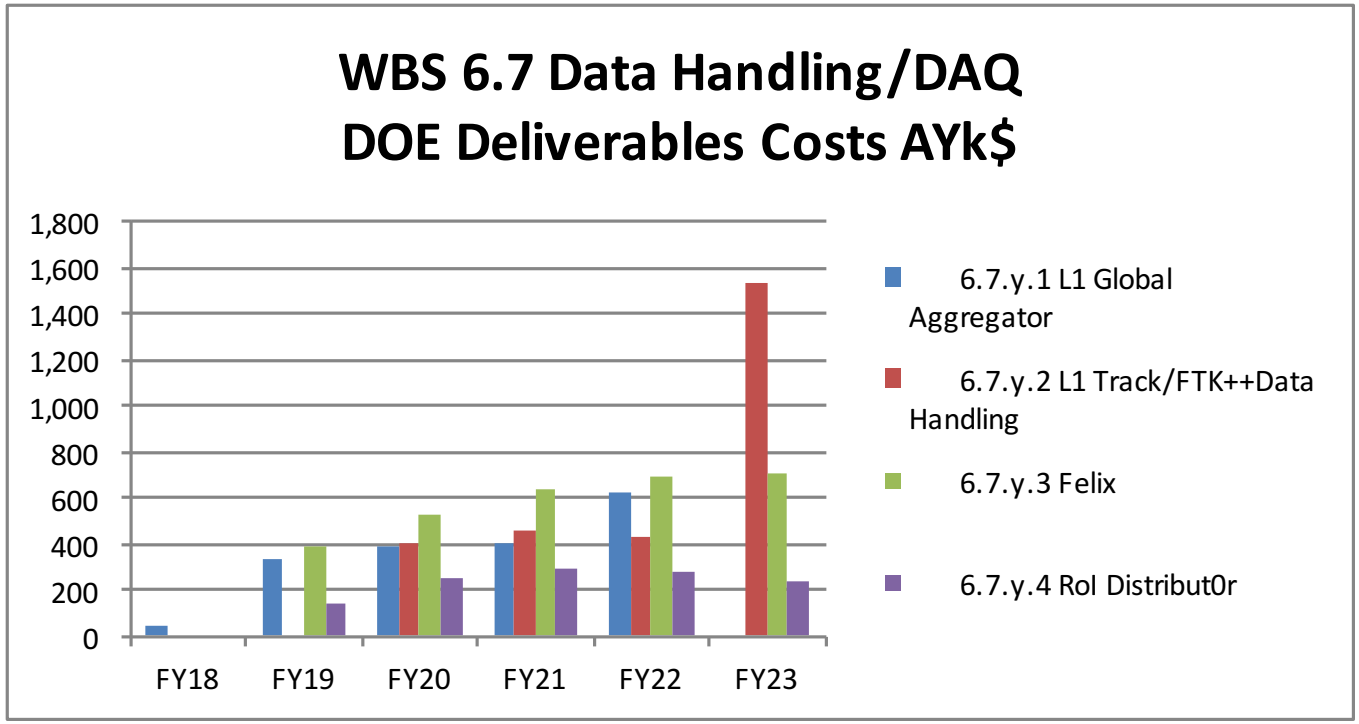


Cost by Phase

6.7 Data Handling/DAQ DOE Level 4 Total Cost (AYk$)								
Item/Phase	**FY18**	**FY19**	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
6.7.y.1 L1 Global Aggregator	**46**	**331**	**393**	**401**	**625**	**0**	**0**	**1,796**
Design	46	0	0	0	0	0	0	46
Prototype		331	393	0	0	0	0	724
Pre-production	0	0	0	401	0	0	0	401
Production	0	0	0	0	625	0	0	625
6.7.y.2 L1 Track/FTK++Data Handling	**0**	**0**	**409**	**463**	**433**	**1,535**	**0**	**2,841**
Design	0	0	409	0	0	0	0	409
Prototype	0	0	0	463	0	0	0	463
Pre-production	0	0	0	0	433	0	0	433
Production	0	0	0	0	0	1,535	0	1,535
6.7.y.3 Felix	**0**	**387**	**528**	**639**	**698**	**710**	**0**	**2,963**
Design	0	387	0	0	0	0	0	387
Prototype		0	528	639	0	0	0	1,167
Production	0	0	0	0	698	710	0	1,408
6.7.y.4 RoI Distribut0r	**0**	**148**	**250**	**289**	**287**	**236**	**0**	**1,211**
Design	0	148	0	0	0	0	0	148
Prototype		0	250	289	0	0	0	540
Production	0	0	0	0	287	236	0	523
DOE Grand Total	**46**	**867**	**1,581**	**1,791**	**2,044**	**2,481**	**0**	**8,811**

Cost Profile

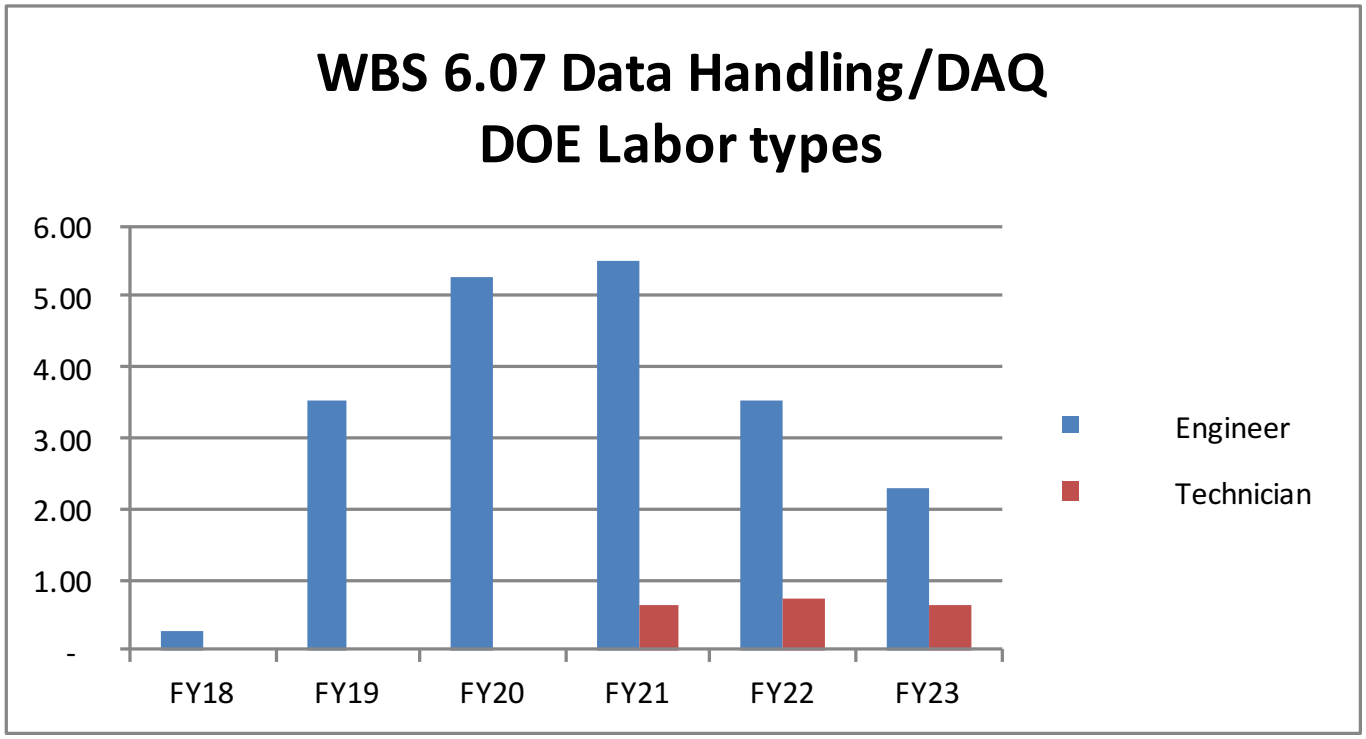
6.7 Data Handling/DAQ DOE Level 4 Total Cost (AYk$)								
Deliverable/Item	**FY18**	**FY19**	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
6.7.y.1 L1 Global Aggregator	46	331	393	401	625	0	0	1,796
6.7.y.2 L1 Track/FTK++Data Handling	0	0	409	463	433	1,535	0	2,841
6.7.y.3 Felix	0	387	528	639	698	710	0	2,963
6.7.y.4 RoI Distribut0r	0	148	250	289	287	236	0	1,211
DOE Total	46	867	1,581	1,791	2,044	2,481	0	8,811



FTE

6.7 Data Handling/DAQ DOE FTEs by Deliverable								
Item/Phase	**FY18**	**FY19**	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Grand Total**
6.7.y.1 L1 Global Aggregator	**0.25**	**1.50**	**1.50**	**1.50**	**1.00**	**-**	**-**	**5.75**
Design	0.25	-	-	-	-	-	-	0.25
Prototype	-	1.50	1.50	-	-	-	-	3.00
Pre-production	-	-	-	1.50	-	-	-	1.50
Production	-	-	-	-	1.00	-	-	1.00
6.7.y.2 L1 Track/FTK++Data Handling	**-**	**-**	**1.00**	**1.13**	**0.75**	**0.63**	**-**	**3.50**
Design	-	-	1.00	-	-	-	-	1.00
Prototype	-	-	-	1.13	-	-	-	1.13
Pre-production	-	-	-	-	0.75	-	-	0.75
Production	-	-	-	-	-	0.63	-	0.63
6.7.y.3 Felix	**-**	**1.55**	**2.00**	**2.50**	**1.80**	**1.80**	**-**	**9.65**
Design	-	1.55	-	-	-	-	-	1.55
Prototype	-	-	2.00	2.50	-	-	-	4.50
Production	-	-	-	-	1.80	1.80	-	3.60
6.7.y.4 RoI Distributor	**-**	**0.50**	**0.75**	**1.00**	**0.75**	**0.50**	**-**	**3.50**
Design	-	0.50	-	-	-	-	-	0.50
Prototype	-	-	0.75	1.00	-	-	-	1.75
Production	-	-	-	-	0.75	0.50	-	1.25
DOE Grand Total	**0.25**	**3.55**	**5.25**	**6.13**	**4.30**	**2.93**	**-**	**22.40**

FTE Profile


WBS 6.07 Data Handling/DAQ
DOE Labor types
6.00
5.00
4.00
3.00
2.00
1.00
-
FY18
FY19
FY20
FY21
FY22
FY23
Engineer
Technician

Risks

- Schedule Risks
  - Late delivery of key components (FPGA etc) and technical decisions; discovery of problems that can only be found in late tests.
  - Mitigation with using schedule contingency; performing detailed tests and applying rigorous performance standards since the early stage
- Cost Risks
  - Discovery of problems may require a new revision of the hardware.
  - Mitigation with adding engineering effort to perform extensive and comprehensive evaluation test to solve all potential issues in early prototypes; using cost contingency
- Technical/Scope Risks
  - Revision of the hardware or increase of the hardware caused by changes introduced by connecting components (L0Topo, L0CTP, AM chip capacity, etc)
  - Mitigation with closely following the development of connecting components and incorporating changes promptly; adding more prototype round; sharing the additional cost with involved international collaborators

Scope Contingency & Opportunity

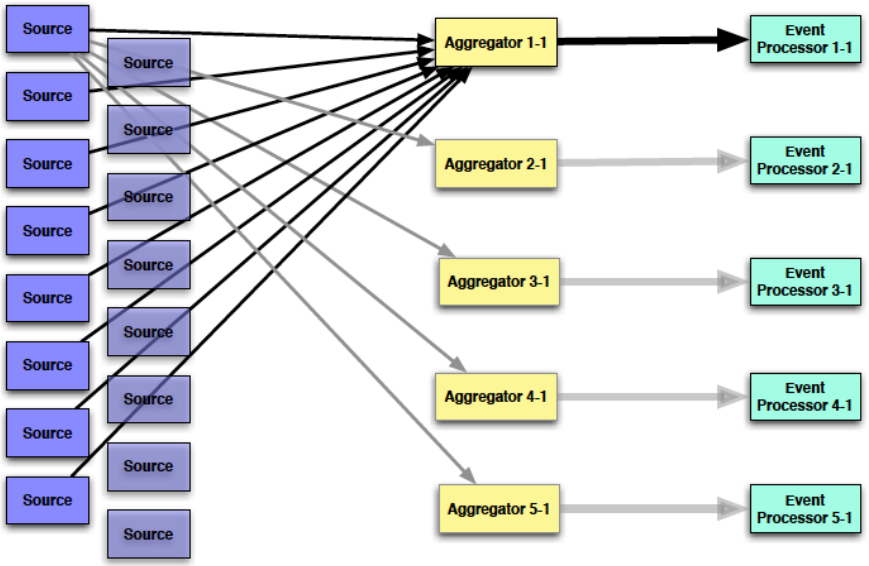
- Scope Contingency
  - Produce only 25% (rather than 50%) of L1Track/FTK++ data handling RTM
    - More contribution needed from ATLAS international institutes, and need be coordinated
- Scope Opportunity
  - Extend to the full production of L1Global Aggregator
    - Beneficial for system QA and project execution
    - Decision by ATLAS TDAQ TDR or later
  - Extend to 30% (rather than 15%) of the FELIX card production
    - Adequate for ITk surface test
    - Decision by ATLAS TDAQ TDR or later

Closing Remarks

- US proposed deliverables for the DAQ/Data Handling scope include L1Global Aggregator, L1Track/FTK++ Data Handling, FELIX and RoI Distributor
- These deliverables are essential to detector readout and trigger input data preparation for ATLAS HL-LHC physics program
- The proposed scope matches well the US expertise and experience in TDAQ
- Total budget for this L2 WBS is $8,811k

6.7.y.1 L1Global Aggregator

- Functionality
  - The Aggregator concentrates information from the detector and trigger systems as a feed-in to a global trigger processing system.
  - The Aggregator board will receive signals from LAr & Til calorimeters, and some trigger systems, then combines the information for transmission to Event Processors.
- Technology approach (as for the scoping document)
  - ATCA boards with high performance FPGAs and high speed optical links

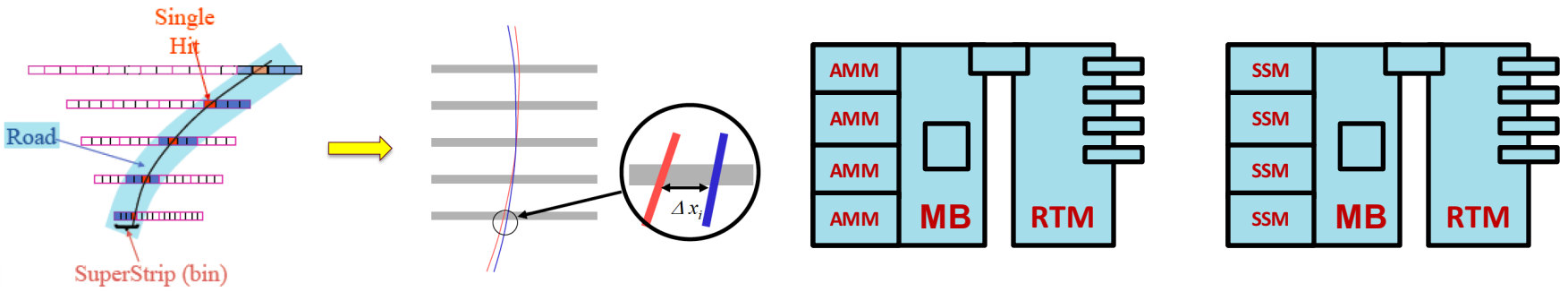


6.7.y.1 L1Global Aggregator

- US deliverable
  - Design and prototype of the Aggregator board
  - Transmission and control firmware
  - Production and testing of 50% of the Aggregator boards (4 of 8)
- Collaboration in work
  - Matching well with US expertise and experience of Phase-I gFEX
  - ATLAS international institutes expressing interests in
    - L1Global Event Processor hardware
    - Production and testing of the rest of the Aggregator boards

6.7.y.2 L1Track/FTK++ Data Handling

- Functionality
  - L1Track and FTK++ planning to use same technologies
    - Associative Memory (AM) chip for pattern match and FPGAs for track fitting
  - L1Track and FTK++ planning to use same hardware
    - Main board holding mezzanine cards
    - Same main board for both AM processing mezzanine and Second Stage Mezzanine
    - High speed data transmission from Rear Transition Module (RTM) to Main board
- Technology approach (as for the scoping document)
  - Data handling focusing on the ATCA RTMs with high speed optical links and firmware to support the data transmission



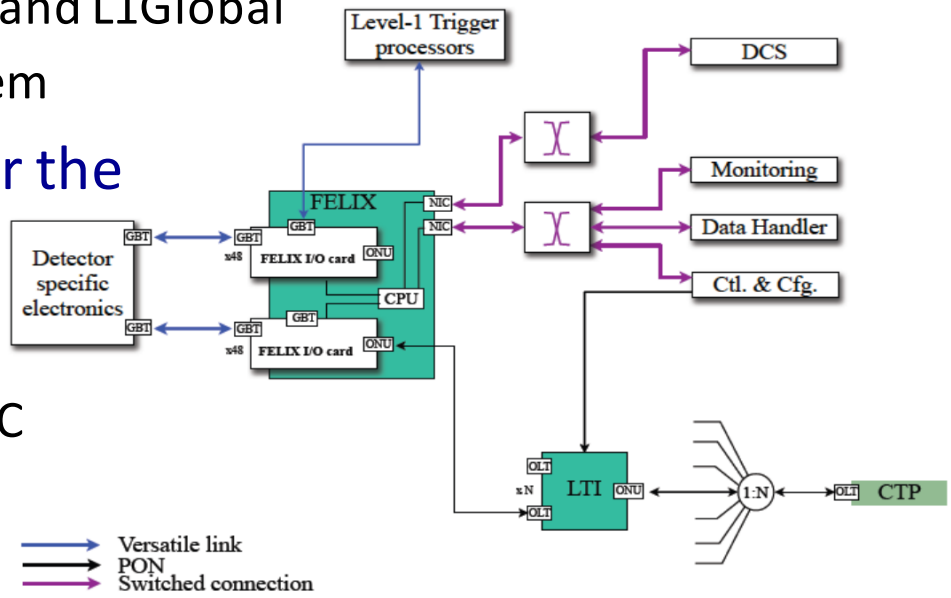
6.7.y.2 L1Track/FTK++ Data Handling

- US deliverable
  - Design and prototype of the RTM
  - Firmware to support data transmission
  - Production and testing of 50% of the RTM boards (697 of 1394)
- Collaboration in work
  - Continuing the work mode for FTK, with ATLAS international institutes contributing to
    - Production and testing of the rest of RTMs

6.7.y.3 FELIX

- Functionality
  - Router between serial/synchronous links and high level network links
  - Detector-agnostic and encapsulating common functionality
  - Handling detector configuration and control of calibration procedures
  - Ensuring connectivity to the detector FE even in case of unavailability of other components (critical for DCS)
  - Low latency links to L1Track and L1Global
  - Interfacing HL-LHC TTC system
- Technology approach (as for the scoping documents)
  - FPGA cards with high

  Performance interconnects in PC

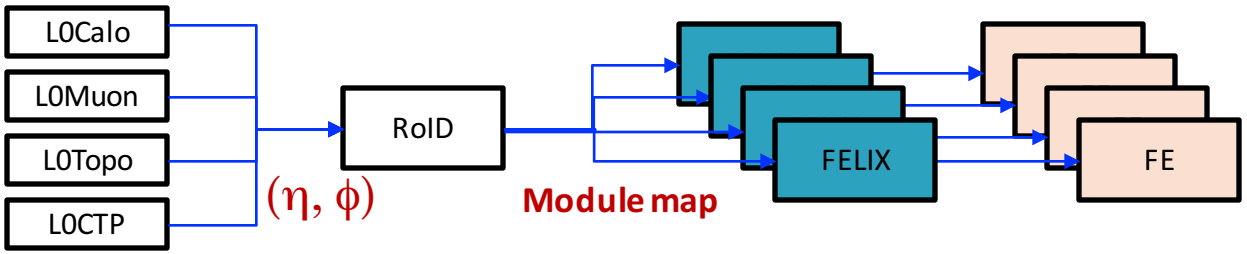


6.7.y.3 FELIX

- US deliverable
  - Design and prototype of the FELIX card
  - Firmware (I/O, TTC/BUSY, etc) development at similar level for Phase-I
  - Production and testing of 15% of the FELIX cards (~70 of 450)
- Collaboration in work
  - Matching well with US expertise and experience of Phase-I FELIX
  - Continuing with the work mode for Phase-I FELIX, with ATLAS international institutes contributing to
    - The rest of firmware and all software
    - Other FELIX hardware components
    - Production and testing of the rest of FELIX cards

6.7.y.4 RoI Distributor

- Functionality
  - RoI Distributor (RoID) receives the complete information about RoIs contributing to accepted trigger elements from L0Calo, L0Muon and L0Topo, and trigger decisions from L0CTP
  - Algorithms in the RoID parse the trigger decision to identify those RoIs requiring processing in the downstream trigger processing systems, and produce the optimal set of RoI information by advanced processing (sorting, merging, overlap removing, etc).
  - In case that the optimal set of RoIs need be sent to detector front-end electronics, RoID will map the RoI information to detector modules.
- Technology approach (as for the scoping document)
  - ATCA boards with high performance FPGAs and high speed links



6.7.y.4 RoI Distributor

- US deliverable
  - Design and prototype of the RoID board
  - Control and processing firmware
  - Production and testing of the full system (2)
- Collaboration in work
  - Unique US expertise and experience
    - Current ATLAS RoIB system solely by US (Design, production, operation and evolution)
  - Encouraged by the ATLAS TDAQ

One-level Hardware Trigger

- ATLAS collaboration wide discussions and studies are ongoing on the possibility to have one-level hardware trigger (L0 @ 1 MHz) rather than the L0/L1 split architecture
- Decision is expected in summer 2016
- In the one-level hardware trigger scenario, nominal L1 work is shifted to HLT/Event Filter
  - L1Global functionality will still be needed but may be performed in different types of hardware
  - Same resource will be needed for both RoI based tracking and full event tracking, so impact to L1Track/FTK++ is small
  - More FELIX cards will be needed to cop the higher rate, but dedicated connections to L1Track and L1Global will no longer be needed
  - RoI Distributor functionality will still be needed but the output will be highly coupled with the CTP output